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Optimization of Empirical Modelling of Advanced Highly Strained $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ pHEMTs for Low Noise Amplifier

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ABSTRACT

An optimized empirical modelling for a 0.25µm gate length of highly strained channel of an InP-based pseudomorphic high electron mobility transistor (pHEMT) using InGaAs–InAlAs material systems is presented. An accurate procedure for extraction is described and tested using the pHEMT measured dataset of I-V characteristics and related multi-bias s-parameters over 20GHz frequency range. The extraction of linear and nonlinear parameters from the small signal and large signal pHEMT equivalent model are performed in ADS. The optimized DC and S-parameter model for the pHEMT device provides a basis for active device selection in the MMIC low noise amplifier circuit designs.

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1. INTRODUCTION

While fabrication process is the key aspect of device production, device modelling becomes essential in understanding the semiconductor device physics, as well as device fabrication process and characterization. Device modelling is utmost importance in analyzing device output characteristics and adequate prediction of device performance. It is now becoming more significant as a cost-effective way to virtually fabricate "Beyond Moore" devices as emphasized in the International Technology Roadmap for Semiconductor (ITRS) 2016 [1]. Modelling allows the designer to understand the semiconductor and its properties by using computational systems so that it accurately reflects the device behaviour. For instance, the empirical device models (EDMs) simulate the external characteristics of devices with equivalent circuits [2]. In addition, accurate modelling is required to predict the linear and nonlinear behaviour of the device and microwave circuit design such as in low noise amplifiers (LNAs) as well as current for the broadband signals [3-6]. By cutting the iteration number of fabrication for device characterization, device modelling reduces the time and cost required for developing a specific device or circuit [7]. The empirical modelling for the pseudormorphic high mobility transistor (pHEMT) sample devices is developed in Agilent's Advance Design System (ADS) software. Practically, it is obtained by optimizing the component values to closely match the measured DC and S-parameters for the device [8]. The extraction of linear and nonlinear parameters from the small and large signal pHEMT equivalent model are presented. Finally, the

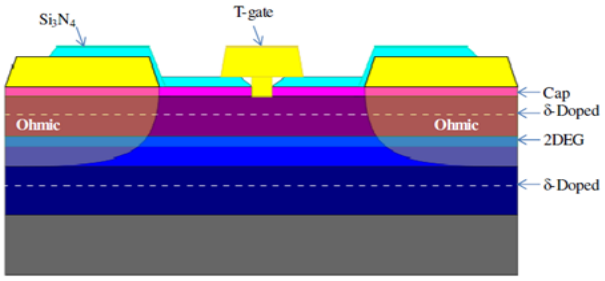
pHEMT model is optimized to be used in the monolithic millimeter wave integrated circuit (MMIC) LNA circuit design.

2. DEVICE EPITAXIAL LAYER

The empirical device modelling presented in this paper is for a 250nm T-gate pHEMT structure which is fabricated by utilizing conventional 1µm i-Line lithography and a novel solvent reflow technique [9]. The XMBE131 pHEMT is a two finger device with 50µm gate width, 250nm gate length and 3µm source-to-drain separation. The strained channel $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ pHEMT device is fabricated with both Pd/Ti/Au gate metallization scheme with conventional thermal evaporation. The epitaxial layer for the XMBE131 pHEMT sample is shown in Figure 1. The structure is made of a thin channel layer and double doping layer to enhance the carrier confinement in the channel. The device pinch off voltage is -1.2 Volt and exhibits great enhancement in the unity current gain frequency, f_T of 90GHz and current drivability (I_{DS}) of 580mA/mm [9].

XMBE131
(Cap) $In_{0.53}Ga_{0.47}As$ 50Å
(Barrier) $In_{0.52}Al_{0.48}As$ 150Å
δ-doped
(Spacer2) $In_{0.52}Al_{0.48}As$ 100Å
(Channel) $In_{0.70}Ga_{0.30}As$ 160Å
(Spacer1) $In_{0.52}Al_{0.48}As$ 100Å
δ-doped
(Buffer) $In_{0.52}Al_{0.48}As$ 4500Å
(Substrate) InP Fe doped

(a)



(b)

Figure 1. (a) Epitaxial layer structures of sample XMBE131 and (b) schematic of in-house fabricated pHEMT sample (Thickness not to scale)

3. PHEMT MODELLING

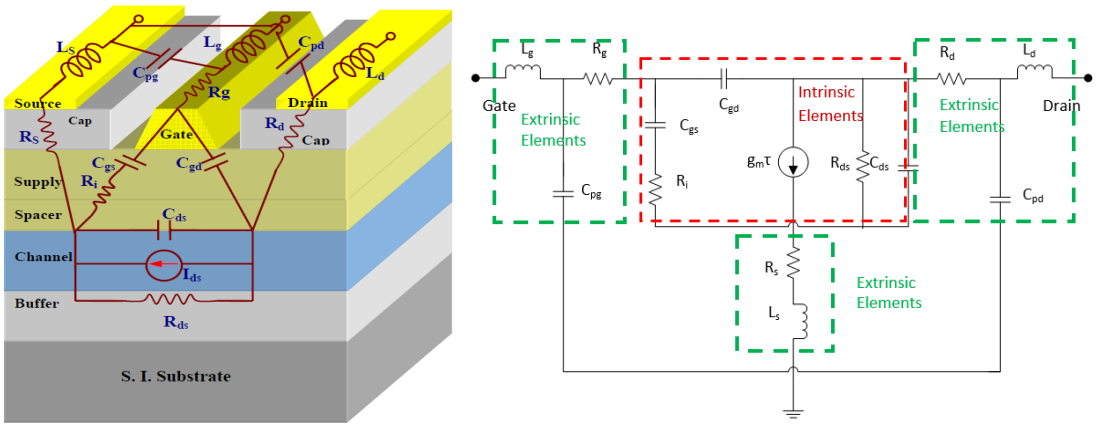
The empirical modelling for the pHEMT device is achieved with the optimization of linear model (small signal model) and nonlinear model (large signal model).

3.1. Linear Model Development

The linear model for HEMTs relates the measured S-parameters with the electrical processes occurring within the device. Figure 2(a) illustrates the conventional HEMT structure with its equivalent small signal model shown in Figure 2(b). The topology in Figure 2 is assumed for building an equivalent circuit model of the device, along with physical correlation to the device; provides an excellent match over a wide frequency range.

The linear model of a HEMT consists of passive devices which can be categorized into intrinsic and extrinsic elements. The model provide advantages to the IC designer to accurately measure S-parameters of the device. The linear model presented in the paper is the most commonly used and followed technique developed by Dambrine *et al*. [11]. Using Agilent Integrated Circuit Characterization and Analysis Program (ICCAP) standard computer-aided design (CAD) tools, the intrinsic and extrinsic parameters were extracted from the measured S-parameter data. The intrinsic model parameters were obtained from hot (active) device bias point, while the extrinsic elements were extracted from the cold (pinched) device measurement [12]. The final element values for linear models were determined by optimization of the initial value to accurately fit the measured data.

The extrinsic parasitic measurements are taken at zero drain bias, V_{DS}=0V and gate voltage below the device pinch-off state, i.e. $V_{GS} < V_p$. The generated initial linear model is optimized by fitting the modelled and measured S-parameter data which will consequently reduce the modelling error. The circuit setup for XMBE131 pHEMT extrinsic element extraction is shown in Figure 3. The two-port network circuit setup was terminated with 50Ω resistance at both input and output port. The measured dataset files from ICCAP is saved in the S2P components. The frequency range is set from 40MHz to 20GHz for the S-parameter simulations.



(a) (b)

Figure 2. HEMT small signal equivalent circuit model [10-11]

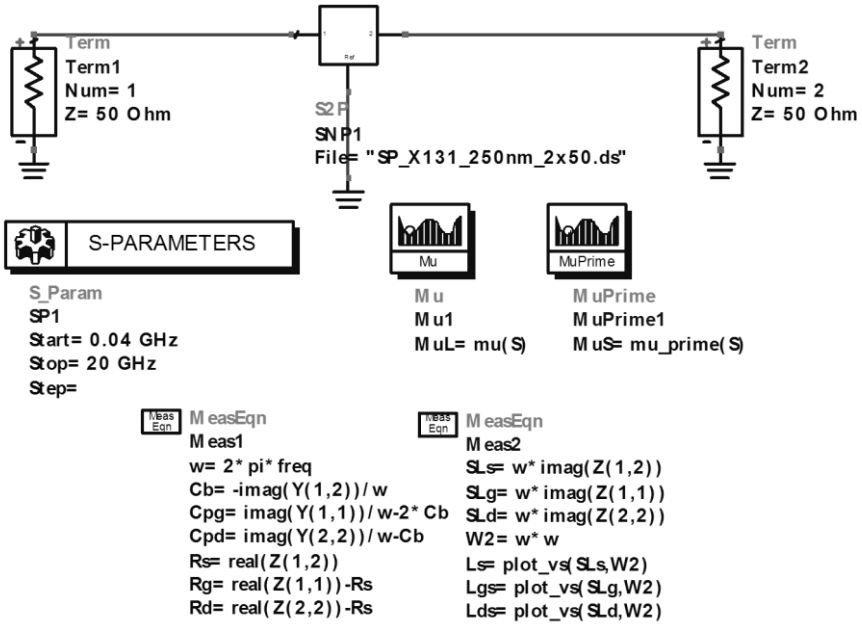


Figure 3. Circuit Setup for extrinsic element extraction (pinched) in ADS for XMBE131

3.2. Nonlinear Model Setup

The nonlinear model consists of optimizing the modelling for the DC and RF characteristics of the device. The parasitic components were extracted from the S-parameter data set measured under different dc current. To develop the DC model, firstly the R_s, R_d and R_g resistances obtained from the linear model are substituted into the ADS EE-HEMT model. The EE-HEMT is an empirical analytic model based on fitting of the measured electrical characteristics of HEMTs. In addition to nonlinear capacitances, the nonlinear element of current functions at the drain-source, gate-source, and gate-drain are dependant on the instantaneous bias conditions (V_{GS} and V_{DS}). As the bias changes, the signal deviates from the static operating point which in turn changes the device's performance characteristics. A relation of current-voltage for the bias conditions is then developed that approximates the measured data.

The EE-HEMT model equations were developed concurrently with parameter extraction techniques to ensure the model parameters was extractable from the measured data. The drain-source parameters and g_m compression parameters are then extracted from the measured g_m versus V_{GS}.These parameters provide the

initial point for the nonlinear device model. The parameters are then tuned for optimum fit between the measured and modelled DC characteristics.

4. RESULTS AND ANALYSIS

4.1. Linear Model

Table 1 tabulated the extrinsic elements of the sample device which are bias independent. These elements are the capacitance, resistance and inductance at the electrodes which results from metallization of the contact with the surface, resistance due to ohmic contact and variation of depletion charge with respect to the gate-source and gate-drain voltages. The gate inductance, L_g is usually large for short gate length devices. The gate resistance is a parasitic element that affects the maximum available gain of a FET, and is inversely proportional to the cross-sectional area of the metal along the gate finger.

It can be observed in Table 1 that the capacitance values increase as the total device width is increased. Since the capacitance value is proportional to the contact area, the capacitance value increases as the contact pad areas become larger. The terminal resistances are also reduced as the device size is increased. For bigger gate width, the total gate area also increases; consequently the terminal resistances are reduced.

Table 1. Extrinsic elements for XMBE131 pHEMT sample device (V_{DS}=1V, I_{DSS} = 20%)

Device size (μm)	C_{pg} (fF)	C_{pd} (fF)	R_S (Ω)	R_g (Ω)	R_d (Ω)	L_S (pH)	L_g (pH)	L_d (pH)
2x50	7.73	6.62	0.69	0.83	0.32	18.70	27.20	23.84
2x200	69.04	24.58	1.81	0.89	1.45	18.91	47.72	61.69

Table 2. Intrinsic parameters for XMBE131 pHEMT sample device (V_{DS}=1V, I_{DSS} = 20%)

Device size (μm)	g_m (mS)	T (psec)	R_i (Ω)	R_{ds} (Ω)	C_{gs} (pF)	C_{ds} (pF)	C_{gd} (pF)
2x50 μm	64.8	1.53	4.33	316.0	0.12	0.01	0.02
2x200 μm	321.8	2.98	2.82	65.6	0.08	0.03	0.03

Intrinsic elements are bias dependant. In Table 2, the capacitance values increase as the total device width increased because the capacitance value is proportional to the contact area. Hence the capacitance increases as the contact pad areas become larger. The terminal resistances increase with increase in device size. As for a larger gate width, the total gate area is increased and consequently it will reduce the terminal resistances [13]. A significant reduction in the resistance between drain and source, R_{ds} values is observed with the increasing of device width. There is a direct correlation between device width increases with the total area increased which consequently reduced the channel resistance.

4.2. Nonlinear Model

The parasitic values implemented in the nonlinear modelling have been shown in the Table 2. Figure 4 shows the experimental (measured) and modelled DC characteristics fitted to each other. The I-V characteristics in Figure 4(a) shows excellent agreement between the two sets of data, except around the kink area. The kink effect is as expected for a short channel device as a result of impact ionization [14]. These show extremely well-behaved curves with a sharply defined pinch-off, a small output conductance and a very small amount of kink effect (indicating little carrier loss under low gate-bias). Nevertheless, for the bias conditions required, the low noise zone in this work (V_{DS} = 1 V) is safely outside the kink region. Figure 4(b) depicts the threshold voltage which shows excellent fitting between measured and the DC empirical model. The curve fitting between the measured and modelled g_m can be observed in Figure 4(c). The model demonstrated a very good agreement between the two data specifically at higher gate voltage, V_{GS}. Nonetheless, there is a marginal divergence at lower V_{GS} due to the limitations in the DC model [15] where kink anomalies are usually observed.

The RF performance is extracted from the nonlinear model simulations. The parameters are tuned and optimized to give an excellent agreement between modelled and measured S-parameter curve. The optimization of parameters are important as to provide a realistic components value which will be considered for the LNA circuit design. Additionally the model is validated via modelling of the S-parameters over several bias points. Moreover, the drain-source currents (I_{DS}) for every bias point are also monitored because

sometimes good matching of S-parameter data can be obtained, although a large difference between modelled and measured I_{DS} values still exists.

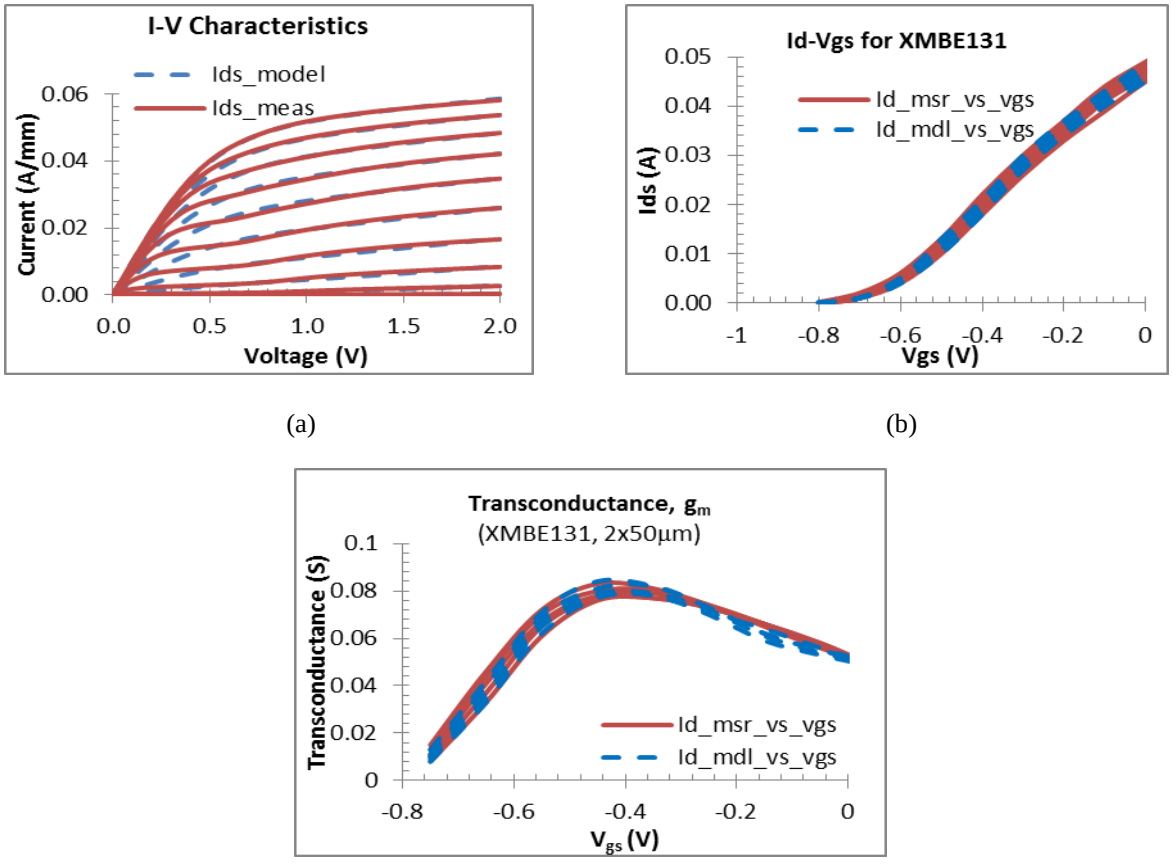


Figure 4. Measured versus modelled XMBE131 pHEMT, (a) I-V characteristics (for V_{GS}=0.1V to -0.8V, -0.1V steps), (b) Threshold voltage (for V_{DS}=1V to 2V, 0.25V steps) and (c) Transconductance (g_m)

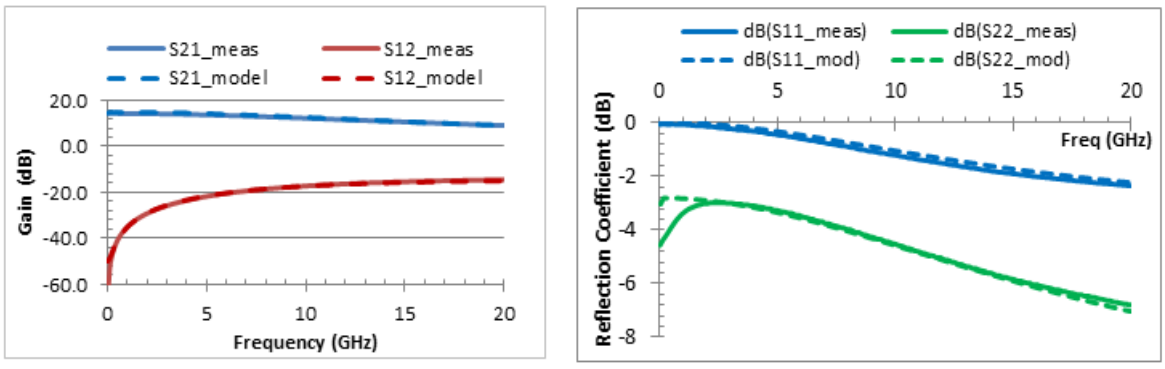


Figure 5. Curve fitting for 2x50µm XMBE131 (a) Forward and Reverse Gain and (b) Input and output reflection coefficient measured at 80% of maximum $g_{m.}$

The biasing point is taken based on the percentage of maximum g_m. In this work, the extracted S-parameter for 80% g_m and 90% g_m bias point (~20% to 30% I_{DSS}) is taken into consideration. The comparison of modelled and measured S-parameter for the nonlinear model of the XMBE131 device is depicted in Figure 5 the frequency range of 40MHz to 20GHz.

The forward gain (S_{21}), reverse gain (S_{12}), input reflection coefficient (S_{11}) and output reflection coefficient (S_{22}) is obtained as illustrated in Figure 5. The gain curve (S21) is about 20dB in the range of 1 ~ 3GHz. The gain starts to decrease with the frequency and the input reflection coefficient (S11) is below -10dB. The modelled data for the bias point show excellent agreement with the measured data with very small percentage errors. The excellent curve fitting in DC and RF characteristics is important in order to obtain an optimized active device. The optimized transistor model presented in Figure 6 is now completed and ready to be implemented in the MMIC LNA circuit design, i.e., in C-band and X-band application.

Figure 6. A Complete transistor model for 2 x 50µm pHEMT sample XMBE131

4.3. Noise Model

The optimized pHEMT device model establish the prediction of the device behaviour, including the noise figure, the important figure of merit (FOM) for an LNA design. The Noise Figure (NF) is a measure of the level of noise generated from an active device when RF signal is applied. The device's minimum noise figure (NF_{min}) is plotted against device width at a certain frequency to analyse the relationship and advantage of device scaling. For optimum device matching, NF_{min} can be viewed as the minimum Noise Figure (NF) that can be produced from the device. Thus, it is important to have optimum RF matching, as improper matching results in a larger noise figure compared to NF_{min}. Fukui's [16] NF_{min} expression is used to find the NF_{min} parameter for the fabricated devices and is derived as in Equation (1) and Equation (2) with a constant, k_1, of 3.5 [17].

$$NF_{\min} = 10 \times \log\left(1 + k_1 \frac{f}{f_T} \sqrt{g_m\left(R_S + R_g\right)}\right) \quad (1)$$

where, f_T is the unity current gain cut-off frequency given by Equation (2).

$$F_T = \frac{g_m}{\left(C_{gs} + C_{gd}\right)} \quad (2)$$

Table 3 represents the minimum noise figure of XMBE131 pHEMT for various frequency of application. This includes calculation of NF_{min} at 2GHz for low frequency, 5.8GHz and 10GHz respectively, for C-band and X-band frequency. The NF_{min} for this sub-micrometer gate length pHEMT are very low as compared to other 1µm gate length devices. Based on Equations (1) – (2), this is due higher f_T in submicron device (usually more than double of the 1µm device f_T). However, the noise figure increases about 50% as

the cut-off frequency doubled. The estimated noise figures are significant for active device selection in the MMIC LNA circuit design [6].

Table 3. Noise performance for fabricated pHEMT devices at V_{DS}=1V, 20% I_{DSS}

Device	g_m (mS)	NF_{min}@ 2GHz (f_T meas)	NF_{min} @ 2GHz (f_T mod)	NF_{min} @ 5.8GHz (f_T_meas)	NF_{min} @ 5.8GHz (f_T_mod)	NF_{min} @ 10GHz (f_T_meas)	NF_{min} @ 10GHz (f_T_mod)
XMBE131 2x50µm	64.80	0.134	0.135	0.379	0.379	0.634	0.635

The g_m, R_s and R_g values are obtained from the optimized linear model. In general, a larger device will exhibit higher noise characteristics. This is anticipated due to the parameter g_m, R_s and R_g in Equation (2). Based on the extrinsic and intrinsic parameter extraction discussed in earlier section, the device's transconductance increases proportional with the increases in the device width. On the other hand, as the device's total width increased, the total of R_s and R_g is reduced. However, the increases in g_m outweigh the decrease in both parasitic values of R_s and R_g. Thus, NF_{min} follows the trend of the square root of g_m, where larger values are obtained for larger devices.

5. CONCLUSION

The empirical models for an advanced highly strained $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ pHEMTs with 0.25µm gate length is developed in ADS using the EEHEMT model. The linear and nonlinear parameters of the small signal and large signal pHEMT equivalent model for the XMBE131 are presented and compared with the experimental results from ICCAP. The DC characteristics and S-parameter acquired from the models are closely matched with the experimental results. Based on the model, the noise figure of the device is calculated at C-band and X-band frequencies to predict the minimum noise figure it might contribute when integrated into an LNA circuit. The optimized nonlinear pHEMT model obtained for XMBE131 pHEMT sample will be used as an active device in the MMIC LNA circuit design.

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